REMARKS

In the action dated September 27, 2004 the Examiner has rejected Claims 1-19 under 35 U.S.C. §102(e) as being anticipated by *Gates,* U.S. Patent Number 5,701,409. As there are only 18 claims in the present application Applicants will consider the Examiner's rejection to be a rejection of Claims 1-18 under 35 U.S.C. §102(e) as being anticipated by *Gates.* That rejection is not well founded and it should be withdrawn.

The claims, as amended in Applicants Preliminary Amendment filed with the Request for Continued Examination (RCE), specify a method and system for simulating a hardware fault on an expansion card by specifying a hardware fault to simulate, determining a particular signal to output utilizing a bus to simulate that hardware fault and thereafter "creating an analog voltage signal representative of said specified hardware fault utilizing a digital-to-analog voltage converter..."

In rejecting Applicants claims the Examiner notes that creating an analog voltage signal representative of the specified hardware fault utilizing a digital-to-analog voltage converter is "inherent to the PCI specification" the Examiner cites the PCI specification § 4.2.5 which specifies pin capacitance and inductance for all pins and output voltage/current curves for switching conditions. This particular portion of the specification also specifies rise/fall slew rates for each output type.

As enumerated by the Board of Patent Appeals and Interferences in the Appeal proceeding this prosecution Applicants now acknowledge that there are inherent analog properties in a digital switching system, such as that specified by a PCI bus; however, Applicants are not now claiming analog voltage versus digital voltage *per se.* Rather, Applicants have expressly claimed the creation of an analog voltage signal representative of a particular specified hardware fault utilizing a digital-to-analog voltage converter and, the Examiner's protestations to the contrary, the mere presence of analog components within a digital switching signal do not suggest the utilization of a digital-to-analog converter. A digital-to-analog converter is a specific type of circuitry and the mere presence of transient analog voltages within a digital circuit system cannot be said to anticipate, show or suggest the utilization of a digital-to-analog converter in the manner set forth within the present claims.

Applicants respectfully urge the Examiner to consider that Applicants do not claim analog voltages *per se* nor do the Applicants merely claim a digital-to-analog converter. Rather, Applicants specifically claim the utilization of a digital-to-analog converter in a particular technique for creating an analog voltage signal which is representative of a specified hardware fault and the references cited by the Examiner are entirely and absolutely bereft of any showing or suggestion of the utilization of a digital-to-analog converter to create an analog voltage signal representative of specified hardware faults in the manner set forth within the claims of the present application.

Applicants note the rejection by the Examiner of Claims 1-18 is an anticipation rejection under 35 U.S.C. §102(e) and the absolute absence of the slightest scintilla of suggestion of the presence of a digital-to-analog converter, let alone the utilization of a digital-to-analog converter to create an analog voltage signal representative of a specified hardware fault is believed to render this rejection unworkable on its face.

Further, addressing the inherent rejection under 35 U.S.C. §103 which is contained within each rejection under 35 U.S.C. §102 and considering the teaching of the PCI local bus specification provided by the Examiner, there is still not the slightest suggestion for the utilization of a digital-to-analog converter to produce an analog voltage signal representative of a specified hardware fault in the manner set forth within the claims of the present application. Consequently, Applicants urge the Examiner to withdraw the rejection of Claims 1-18 under 35 U.S.C. §102(e) as that rejection is unlikely to be sustained.

In conclusion, Applicants urge the Examiner to consider page 6 of the decision of the Board of Patent Appeals and Interferences in the appeal in this application in which the Examiner was commended by the Board for correctly noting that a digital-to-analog converter was not claimed and the Board then stated "If it was, the Examiner would then have tried to find prior art to show the obviousness of using a DAC in place of a logic gate." Despite the direction of the Board of Patent Appeals and Interferences the Examiner has made no such showing and consequently Applicants urge that the rejection of Claims 1-18 is not well founded and it should be withdrawn.

CONCLUSION

No additional fees are believed to be necessary, however, in the event that any additional fees are required, please charge those fees and any other required fees to **IBM Corporation Deposit Account Number 09-0449.** No extension of time is believed to be required; however, in the event an extension of time is required please consider the extension requested and charge those fees to **IBM Corporation Deposit Account Number 09-0449.**

Respectfully submitted,

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